REMARKS

The Applicant thanks the Examiner for the careful examination of this application and respectfully requests the entry of the amendments indicated hereinabove.

Claims 30-34 are pending. Claims 30, 31, and 34 are rejected and Claims 32-33 are objected to. Claims 30 and 34 are amended hereinabove.

Independent Claim 30 positively recites a nitrided dielectric between the silicon nitride encapsulation layer and the gate dielectric sidewall. Claim 30 also positively recites sidewall spacers coupled to the silicon nitride encapsulation layer. These advantageously claimed features are not taught or suggested by the patents granted to San et al. or Tseng; either alone or in combination.

San et al. does not teach the advantageously claimed invention because San et al. does not teach a transistor structure having a nitrided dielectric, a nitride encapsulation layer, and sidewall spacers as advantageously claimed. Rather, San et al. teaches a transistor structure having just sidewall bodies and a nitride encapsulation layer (column 5 lines 25-26 and 49-50, FIG. 2b).

Moreover, San et al. does not teach the advantageously claimed invention because San et al. does not teach a nitrided dielectric between the silicon nitride encapsulation layer and the gate dielectric sidewall (FIG. 2b, note the thickness of the titanium silicide layers 86, 88 as discussed in column 5 lines 47-48).

Similarly, Tseng does not teach the advantageously claimed invention because Tseng does not teach a transistor structure having a nitrided dielectric, a nitride encapsulation layer, and sidewall spacers as advantageously claimed. Rather, Tseng teaches a transistor structure having just insulator spacers (column 3 lines 23-29, FIG. 2). Therefore, Tseng does not teach the advantageously claimed invention because Tseng does not teach either a silicon nitride encapsulation layer or a nitrided dielectric between the silicon nitride encapsulation layer and the gate dielectric sidewall (FIGS. 2-4, column 3 lines 23-50).

The Applicant respectfully traverses the assertion in the Office Action that it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of San et al. with the teachings of Tseng. The Applicant submits that one of ordinary skill in the art would not combine flash or UV EPROM teachings (San et al., column 4 lines 1-4) with MOSFET teachings (Tseng, column 3 lines 35-42). Furthermore, San et al. teaches away from being combined with the teachings of Tseng because of the problems inherent in the use of silicon nitride layers formed with the conventional manufacturing techniques of

Tseng in column 3 lines 23-30 of Tseng (see San et al., column 1 lines 31-45, column 4 lines 2-41, and column 5 lines 52-57). Moreover, one of ordinary skill in the art would not combine the teachings of San et al. into Tseng because the expensive silicon nitride deposition processes taught by San et al. (column 4 lines 17-41) would render the MOSFETs of Tseng uncompetitive in the marketplace (i.e. due to the higher price point).

For the foregoing reasons, the Applicant respectfully traverses the rejection of Claim 30 and respectfully asserts that Claim 30 is patentable over the patents granted to San et al. and Tseng; either alone or in combination. Furthermore, Claims 31-33 are allowable for depending on allowable independent Claim 30 and, in combination, including limitations not taught or described in the references of record.

Independent Claim 34 positively recites a nitrided dielectric between the silicon nitride encapsulation layer and the gate dielectric at the sidewall. These advantageously claimed features are not taught or suggested by the patents granted to San et al. or Tseng; either alone or in combination.

San et al. does not teach the advantageously claimed invention because San et al. does not teach a transistor structure having a nitrided dielectric, a nitride encapsulation layer, and sidewall spacers as advantageously claimed. Rather, San et al. teaches a transistor structure having just sidewall bodies and a nitride encapsulation layer (column 5 lines 25-26 and 49-50, FIG. 2b).

Moreover, San et al. does not teach the advantageously claimed invention because San et al. does not teach a nitrided dielectric between the silicon nitride encapsulation layer and the gate dielectric sidewall (FIG. 2b, note the thickness of the titanium silicide layers 86, 88 as discussed in column 5 lines 47-48).

Similarly, Tseng does not teach the advantageously claimed invention because Tseng does not teach a transistor structure having a nitrided dielectric, a nitride encapsulation layer, and sidewall spacers as advantageously claimed. Rather, Tseng teaches a transistor structure having just insulator spacers (column 3 lines 23-29, FIG. 2). Therefore, Tseng does not teach the advantageously claimed invention because Tseng does not teach either a silicon nitride encapsulation layer or a nitrided dielectric between the silicon nitride encapsulation layer and the gate dielectric sidewall (FIGS. 2-4, column 3 lines 23-50).

The Applicant respectfully traverses the assertion in the Office Action that it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of San et al. with the teachings of Tseng. The Applicant submits that one of ordinary skill in the art would not combine flash or UV EPROM teachings (San et al., column 4 lines 1-4) with MOSFET teachings

(Tseng, column 3 lines 35-42). Furthermore, San et al. teaches away from being combined with the teachings of Tseng because of the problems inherent in the use of silicon nitride layers formed with the conventional manufacturing techniques of Tseng in column 3 lines 23-30 of Tseng (see San et al., column 1 lines 31-45, column 4 lines 2-41, and column 5 lines 52-57). Moreover, one of ordinary skill in the art would not combine the teachings of San et al. into Tseng because the expensive silicon nitride deposition processes taught by San et al. (column 4 lines 17-41) would render the MOSFETs of Tseng uncompetitive in the marketplace (i.e. due to the higher price point).

For the foregoing reasons, the Applicant respectfully traverses the rejection of Claim 34 and respectfully asserts that Claim 34 is patentable over the patents granted to San et al. and Tseng; either alone or in combination.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

Rose Alyssa Keagy
Attorney for Applicant
Reg. No. 35,095

Texas Instruments Incorporated
PO BOX 655474, M/S 3999
Dallas, TX 75265
Telephone-972/917-4167; FAX - 972/917-4409/4418